REMARKS

Claims 1-27 are currently pending in the application. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

Allowed Claims

Applicant appreciates the indication that claim 20 contains allowable subject matter. However, Applicant submits that all of the claims are in condition for allowance for the following reasons.

35 U.S.C. § 102 Rejection

Claims 1-3, 5-7, 9, 12-19, 21, 22 and 24-27 were rejected under 35 U.S.C. § 102(e) for being anticipated by U. S. Patent No. 6,747,471 issued to Chen (hereinafter, "CHEN"). This rejection is respectfully traversed.

To reject a claim under 35 U.S.C. §102, a single prior art reference must contain each and every limitation of the claim, either expressly or under the doctrine of inherency. Constant v. Advanced Micro-Devices, Inc. , 848 F.2d 1560, 1570 (Fed. Cir.), cert. denied, 488 U.S. 892 (1988). Applicant submits that CHEN does not disclose every feature of the claimed invention.

Independent Claims 1, 15, 21 and 27

The present invention generally relates to kerf design processing during semiconductor chip design processing, and to coordinating kerf design and chip design processes.

Claim 1 recites, in relevant part:

generating kerf data corresponding to the chip data; and
manipulating the kerf data by use of kerf processing using a same
manipulation process as for the chip data.

Claim 15 recites, in relevant part:

creating and manipulating kerf design data concurrently with chip data
design manipulation processing by using same parameters in the kerf design
data manipulation and chip data design manipulation thereby ensuring that the
kerf design data and the chip design data are consistent.

Claim 21 recites, in relevant part:

a component to generate kerf data corresponding to the chip data; and
a component to manipulate the kerf data via kerf processing using the
same manipulation process as the chip data.

Claim 27 recites, in relevant part:

a second computer program code to generate kerf data corresponding to
the chip data; and
a third computer program code to manipulate the kerf data via kerf
processing using the same manipulation process as the chip data.

The Examiner asserts that CHEN shows all the elements of independent claims

1, 15, 21, and 27. (Abstract, col. 1, line 63 – col. 2, line 14, col. 3, lines 35 – 65, col. 6,

lines 35 – 60 and col. 13, lines 55 – 65). Applicants respectfully disagree.

First, the Examiner asserts that CHEN discloses generating kerf data

corresponding to the chip data (col. 3, lines 35 – 55). Applicant respectfully disagrees.

CHEN provides a method and apparatus for estimating burn-in time for integrated

circuits employing a reliability testing structure placed in a scribe line area of a wafer to

permit improved estimation of burn-in time for integrated circuits on a wafer.

Specifically, CHEN discloses forming testing structures in the kerf area, each testing

structure having multiple evaluation devices. Applicant submits that CHEN is silent as

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to any method for generating kerf data. Rather, CHEN discloses forming kerf testing structures. Therefore, CHEN fails to disclose a method of generating kerf data corresponding to the chip data. Accordingly, CHEN does not show all of the features of the claimed invention.

Second, the Examiner asserts that CHEN discloses a method including manipulating the kerf data by use of kerf processing using a same manipulation process as for the chip data (col. 6, lines 35-58). Specifically, the Examiner notes that CHEN discloses various testing devices and circuits that may be formed in the kerf area, and asserts that these devices require the same manipulation process as the chip data. Applicant respectfully disagrees.

Even assuming *arguendo* that CHEN discloses a method of generating kerf data corresponding to the chip data, which Applicant does not concede, CHEN does not disclose, at col. 6, lines 35-58, a method for manipulating the kerf data by use of kerf processing using the same manipulation process as for the chip data.

In the method disclosed in CHEN, the various devices and circuits that make up the testing structures formed in the kerf area include: ring oscillator circuits, capacitor dielectric film evaluation devices, gate oxide integrity devices, polycrystalline silicon heating devices, contact metallurgy evaluation chains, interlayer via chains, MOS evaluation devices, plasma etching antenna affect patterns, metal electromigration structures, and input/output pad structures. These testing devices are created to permit evaluation of failure mechanisms of the integrated circuit. However, CHEN is silent as to how any kerf data is processed. Furthermore, CHEN is silent as to any chip data and a chip data manipulation process. Additionally, CHEN is silent as to structures present

on the chip, and certainly does not disclose that the testing structures formed in the kerf area of the wafer are the same structures that are also present on the chips formed from the wafer (as the Examiner seems to suggest). In fact, if there is to be an interpretation, the disclosure of CHEN forming the listed testing devices in the kerf area, teaches away from manipulating kerf data using the same manipulation process as that used for the chip data. Thus, CHEN does not teach, at col. 6, lines 10-25, manipulating the kerf data by use of kerf processing using a same manipulation process as for the chip data. Accordingly, CHEN does not show all of the features of the claimed invention.

In addition, Applicants respectfully submit that CHEN does not show creating and manipulating kerf design data concurrently with chip data design manipulation processing, as recited in claim 15. As discussed above, CHEN is directed to forming testing structures in the kerf area for improved estimation of burn-in time for an integrated circuit on a wafer. CHEN is silent as to any manipulation of kerf design data, and is silent as to a chip data design manipulation processing. Therefore, CHEN does not show all of the features of the claimed invention.

Accordingly, Applicant respectfully requests that the rejection over claims 1, 15, 21 and 27 be withdrawn.

Dependent Claims 2, 3, 5-7, 9, 12-14, 16-19, 22 and 24-26

Claims 2, 3, 5-7, 9, 12-14, 16-19, 22 and 24-26 are dependent claims, depending from respective distinguishable base claims. Accordingly, these claims should also be in condition for allowance based upon their dependencies. Accordingly, Applicant

respectfully requests that the rejection over claims 2, 3, 5-7, 9, 12-19, 22 and 24-26 be withdrawn.

35 U.S.C. § 103 Rejection

Claims 4, 10, 11, and 23 were rejected under 35 U.S.C. § 103(a) for being unpatentable over CHEN in view of Chiang et al. "From CIF to Chips," 1989 IEEE Eighth Biennial University/Government/Industry Symposium Proceedings (hereinafter, "CHIANG"). Additionally, claim 8 was rejected under 35 U.S.C. § 103(a) for being unpatentable over CHEN in view of U.S. patent No. 6,330,708 issued to Parker et al. (hereinafter, "PARKER"). These rejections are respectfully traversed.

Claims 4, 10, 11, and 23 are dependent claims, depending from distinguishable base claims. Accordingly, these claims should also be in condition for allowance by virtue of their dependencies. Additionally, it is submitted that CHIANG also does not compensate for the deficiencies in CHEN, and accordingly does not show the features of at least claims 1, 15, and 21. For example, CHAING shows a method for combining a number of students' IC designs onto a single multi-project wafer, to decrease the time required for fabrication. CHAING is silent as to generating kerf data, kerf processing and kerf data corresponding to chip data.

Claim 8 is a dependent claim, depending from a distinguishable base claim. Accordingly, this claim should also be in condition for allowance by virtue of its dependency. Additionally, it is submitted that PARKER also does not compensate for the deficiencies in CHEN, and accordingly does not show the features of at least claim 1. For example, PARKER shows a method for producing CATS include files. PARKER

does not disclose that kerf data is manipulated by the use of kerf processing using the same manipulation process as for the chip.

Accordingly, Applicants respectfully request that the rejection over claims 4, 8, 10, 11, and 23 be withdrawn.

CONCLUSION

In view of the foregoing remarks, Applicant submits that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,
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